REMARKS

In the present application, claims 1-44 are pending. Claims 1-44 were rejected. Claims 2, 4, 19, 20, 25, 40, and 41 have been amended. No new matter has been added. As a result of this response, claims 1-44 are believed to be in condition for allowance.

Drawings

The Examiner objected to the drawings asserting that "they include the following reference character(s) not mentioned in the description: Element 22A of figure 4. It is acknowledged that reference to element 22a is made in the specification but it is not explicitly stated." The specification is amended herein to correct the inadvertent references to "decode stage 22" to read as "decode stage 22A" as clearly referenced in Fig. 4.

Claim Objections

The Examiner objected to claims 4 and 25 because of an informality. Claims 4 and 25 are amended herein in accordance with the Examiner's suggestion to correct the informality. As a result, Applicants respectfully traverse the objections to claims 4 and 25.

Claim Rejections – 35 USC § 112

The Examiner rejected claims 2 as providing insufficient antecedent basis for the limitation "said program instructions." The Examiner further rejected claims 7-8 because of their dependency on claim 2. Claim 2 is amended to herein to remove the reference to "program instructions" and to more clearly recite "at least one instruction word and said extension to said at least one instruction word" in lieu thereof. As a result, claim 2 is in condition for allowance. As claims 7-8 depend upon claim 2, they are likewise in condition for allowance.

The Examiner rejected claim 20 as providing insufficient antecedent basis for the limitation "said at least one extension". Claim 20, as well as claim 19, has been amended to make clear that "said extension to said at least one instruction word has a width of 8-bits." As a result of this amendment, claim 20 is believed to be in condition for allowance. As

claim 21 was rejected because of its dependency on claim 20, claim 21 is likewise in condition for allowance. The Examiner rejected claim 41 for reciting "said at least one extension" for the reasons noted above with respect to claim 20. For the reasons discussed above, claims 40 and 41 have been likewise amended and are believed to be in condition for allowance. The Examiner further rejected claim 42 because of its dependency on claim 41. For the reasons discussed above, claim 42 is likewise in condition for allowance.

Claim Rejections – 35 USC § 102(b)

The Examiner rejected claims 1-44 as being anticipated by Yates. Jr. et al (U.S. Patent No. 6,397,379 B1), hereinafter referred to as "Yates et al.". Specifically, with respect to claim 1, the Examiner asserted that Yates et al. disclose "a digital data processor (see column 3, lines 14-15: Same as microprocessor) comprising an instruction unit (See column 3, lines 15-20), said instruction unit comprising a code page (See column 73, lines 28-30: Discloses the existence of code pages) that is partitioned for storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to at least one instruction word (see column 2, lines 33-36 and column 3, lines 15-20: The instruction unit can operate with two sources of instructions and pages can be partitioned to handle two sets of instructions)."

The standard for anticipation under 35 USC §102 is one of strict identity. To anticipate a claim for patent, a single prior source must contain all of the claim's elements. (See *Herman v. William Brooks Shoe Co.*, 54 USPQ2d 1046 (S.D. N.Y. 2000)). Applicants respectfully disagree with the Examiner's characterization of Yates et al. Specifically, Applicants assert that Yates et al. do not teach a code page partitioned for storing a plurality of instruction words in a first section and an extension to at least one instruction word in a second section as claimed.

Claim 1 recites:

> 1. A digital data processor comprising an instruction unit, said instruction unit comprising a code page that is partitioned for storing in a first section thereof a

plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word.

At the Examiner's citation of col. 2, lines 33-36, it is stated, "The memory is divided into pages for management by a virtual memory manager. The program is coded in instructions of the first and second instruction sets and uses first and second data storage conventions." There is further stated, "The switch is responsive to a first flag value stored in each table entry, and controls the instruction processor to interpret instructions under, alternately, the first or second instruction set as directed by the first flag value of the table entry corresponding to an instruction's memory page. The transition handler is designed to recognize when program execution has transferred from a page of instructions using the first data storage convention to a page of instructions using the second data storage convention, as indicated by the second flag values stored in table entries corresponding to the respective pages ..." At the Examiner's citation of col. 3, lines 15-20, it is stated, "An instruction unit of the chip is configured to fetch instructions managed by the virtual memory manager, and configured to execute instructions coded for first and second different computer architectures or coded to implement first and second different data storage conventions."

As is evident, Yates et al. teaches a program coded using two different instruction sets wherein each instruction set is stored using one of two storage conventions. A table holds two flag values for each memory page. A first flag value defines which of the two instruction sets is used on the memory page while the second flag indicates which of the two storage conventions is used on the memory page. Each of the flags applies to an entire memory page. The Examiner's assertion that "pages can be partitioned to handle two sets of instructions" can be interpreted congruent with the teachings of Yates et al. if the assertion is understood to state that many pages are partitioned **on a per page basis** such that each page can handle one, and only one, of two instruction sets. As the flags indicate, each page is wholly coded using a single instruction set and a single storage convention.

In contrast, claim 1 recites "**a** code page that is partitioned for storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word." (emphasis

added) As is clearly evident, claim 1 recites that a code page is partitioned into a first and second section. Yates et al. do not teach that a code page can be partitioned into two sections as claimed. Rather, as discussed above, each page of Yates et al. is entirely comprised of one instruction set stored using a single storage convention. There is no partitioning of a page of Yates et al.

In addition, claim 1 recites that a plurality of instruction words is stored in the first section and an extension to at least one instruction word is stored in the second section. Yates et al. do not disclose that the "instructions of the first and second instruction sets" are anywhere represented as an instruction and a separately stored extension to the instruction. Rather, Yates et al. teach that each instruction is coded twice, specifically "for first and second different computer architectures".

Yates et al. therefore fail to teach numerous elements recited in claim 1 and discussed above. For these reasons alone, claim 1 is in condition for allowance. As all of claims 2-21 depend upon claim 1, they are likewise in condition for allowance. Independent claim 22 is drawn to a method similarly incorporating the recited elements of claim 1 discussed above. For the reasons discussed above with reference to claim 1, claim 22 is likewise in condition for allowance. As all of claims 23-42 depend upon claim 22, they are likewise in condition for allowance. Independent claim 43 is drawn to a computer program similarly incorporating the recited elements of claim 1 discussed above. For the reasons discussed above with reference to claim 1, claim 43 is likewise in condition for allowance. As claim 44 depends upon claim 43, claim 44 is likewise in condition for allowance.

While all of claims 1-44 are therefore in condition for allowance, Applicants respectfully note the following. With regards to claim 3, the Examiner asserts that Yates et al. disclose at least one page table entry bit having a state for indicating, on a code page by code page basis, whether the code page is partitioned into said first and second sections or is comprised of a single section storing only instruction words. The Examiner cites as support co. 2, lines 36-49 of Yates et al. as support for the assertion while stating "There are flags for both switching from one set of instructions to another and from one storage section to another." The Examiner is incorrect in asserting that Yates et al. disclose switching "from one storage section to another". Rather, as discussed above, Yates et al. disclose switching

from one data storage convention to another. As a result, Yates et al. does not disclose a page table entry bit for indicating, on a code page by code page basis, whether the code page is partitioned into said first and second sections or is comprised of a single section storing only instruction words as recited in claim 3. For this additional reason claim 3 is in condition for allowance.

With regards to claim 6, the Examiner cites col. 61, lines 15-20 of Yates et al. as disclosing the "address circuitry for addressing an instruction word in said first section using a current instruction address, while simultaneously addressing an extension to said instruction word at a fixed offset from said current instruction address" recited in claim 6. Specifically, the Examiner asserts that Yates et al. disclose that "Instructions and an offset can be accessed at the same time." Without addressing the correctness of the Examiner's assertion, it is clear that Yates et al. do not disclose addressing **an extension to** an instruction word at an offset as claimed. As discussed above, Yates et al. does not disclose extensions to instruction words, much less a manner of addressing such extensions. For this additional reason claim 6 is in condition for allowance.

Claim 9 recites "an address comparator for detecting when program execution has reached the end of the first section for ensuring that a next instruction address is not contained in the second section." The Examiner again cites col. 2, lines 36-51 while asserting that "There are flags for switching from one storage section to another and there is available information on the data in the storage sections." As discussed above, Yates et al. disclose no such thing. Specifically, Yates et al. disclose a flag for switching program execution from "a page of instructions using the first data storage **convention** to a page of instructions using the second data storage **convention**." (emphasis added). Yates et al. does not disclose sections of a page and the disclosed switching is between data **storage conventions**, not storage sections. For this additional reason claim 9 is in condition for allowance.

Applicants note that claims 24, 27, and 30 recite elements similar to those of claims 3, 6, and 9, respectively. For the additional reasons discussed above, claims 24, 27, and 30 are likewise in condition for allowance.

The Examiner is respectfully requested to reconsider and remove the rejections of the claims under 35 U.S.C. 102(b) based on Yates et al., and to allow all of the pending claims 1-

44 as now presented for examination. An early notification of the allowability of the pending claims is earnestly solicited.

Respectfully submitted:

15 June 06

Jeffrey R. Ambroziak Date

Reg. No.: 47,387

Customer No.: 29683

HARRINGTON & SMITH, LLP

4 Research Drive

Shelton, CT 06484-6212

Telephone: (203)925-9400

Facsimile: (203)944-0245

email: hsmith@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

6-15-06 Ann Okrentowich

Date Name of Person Making Deposit